Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-162 (Cancelled)

163. (Currently amended) A chip package comprising:

a ~~first insulating~~ die-surrounding layer;

a die between a first portion of said ~~first insulating~~ die-surrounding layer and a second portion of said ~~first insulating~~ die-surrounding layer, wherein said die has a top surface substantially coplanar with a top surface of said ~~first insulating~~ die-surrounding layer;

a ~~second insulating~~ first dielectric layer on said top surface of said die and said top surface of said ~~first insulating~~ die-surrounding layer;

a patterned metal layer over said ~~second insulating~~ first dielectric layer, said top surface of said die and said top surface of said ~~first insulating~~ die-surrounding layer, wherein said patterned metal layer is connected to said die through an opening in said ~~second insulating~~ first dielectric layer;

a comb-shaped capacitor over said ~~second insulating~~ first dielectric layer; and

a ~~third insulating~~ second dielectric layer on said patterned metal layer and said comb-shaped capacitor, and over said ~~second insulating~~ first dielectric layer, said top surface of said die and said top surface of said ~~first insulating~~ die-surrounding layer.

164. (Currently amended) The chip package in claim 163, wherein said comb-shaped capacitor comprises a portion vertically over said first portion of said ~~first insulating~~ die-surrounding layer.

165. (Cancelled)

166. (Currently amended) The chip package in claim 163, wherein said ~~second insulating~~ first dielectric layer comprises polyimide.

167. (Currently amended) The chip package in claim 163, wherein said ~~second insulating~~ first dielectric layer comprises benzocyclobutene (BCB).

168. (Previously presented) The chip package in claim 163, wherein said patterned metal layer comprises electroplated copper.

169. (Currently amended) The chip package in claim 163, wherein said ~~third insulating~~ second dielectric layer comprises polyimide.

170. (Currently amended) The chip package in claim 163, wherein said ~~third insulating~~ second dielectric layer comprises benzocyclobutene (BCB).

171. (Previously presented) The chip package in claim 163 further comprising multiple solder bumps configured for external connection.

172. (Cancelled)

173. (Previously presented) The chip package in claim 163 further comprising multiple gold bumps configured for external connection.

174-175. (Cancelled)

176. (Currently amended) The chip package in claim 163 further comprising a substrate under said die and under said first and second portions of said ~~first insulating~~ die-surrounding layer.

177. (Currently amended) The chip package in claim 176, wherein said substrate comprises a silicon substrate.

178. (Currently amended) The chip package in claim 163, wherein said ~~first insulating~~ die-surrounding layer comprises [[an]] epoxy.

179. (Currently amended) A chip package comprising:

a ~~first insulating~~ die-surrounding layer;

a die between a first portion of said ~~first insulating~~ die-surrounding layer and a second portion of said ~~first insulating~~ die-surrounding layer, wherein said die has a top surface substantially coplanar with a top surface of said ~~first insulating~~ die-surrounding layer;

a ~~second insulating~~ first dielectric layer on said top surface of said die and on said top surface of said ~~first insulating~~ die-surrounding layer;

a patterned metal layer over said ~~second insulating~~ first dielectric layer, said top surface of said die and said top surface of said ~~first insulating~~ die-surrounding layer, wherein said patterned metal layer is connected to a first metal pad of said die through a first opening in said ~~second insulating~~ first dielectric layer, and wherein said patterned metal layer is connected to a second metal pad of said die through a second opening in said ~~second insulating~~ first dielectric layer, wherein said first metal pad is connected to said second metal pad through said patterned metal layer; and

a passive device over said ~~second insulating~~ first dielectric layer.

180. (Currently amended) The chip package in claim 179, wherein said ~~first insulating~~ die-surrounding layer comprises an epoxy.

181. (Previously presented) The chip package in claim 179 further comprising multiple solder bumps configured for external connection.

182. (Currently amended) The chip package in claim 179, wherein said ~~second insulating~~ first dielectric layer comprises polyimide.

183. (Currently amended) The chip package in claim 179, wherein said ~~second insulating~~ first dielectric layer comprises benzocyclobutene (BCB).

184. (Currently amended) The chip package in claim 179 further comprising a ~~third insulating~~ second dielectric layer on said patterned metal layer and said passive device, and over said ~~second~~

~~insulating~~ first dielectric layer, said top surface of said die and said top surface of said ~~first insulating~~ die-surrounding layer.

185. (Currently amended) The chip package in claim 184, wherein said ~~third insulating~~ second dielectric layer comprises polyimide.

186. (Currently amended) The chip package in claim 184, wherein said ~~third insulating~~ second dielectric layer comprises benzocyclobutene (BCB).

187. (Previously presented) The chip package in claim 179, wherein said patterned metal layer comprises a ground bus connecting said first metal pad to said second metal pad.

188. (Previously presented) The chip package in claim 179, wherein said patterned metal layer comprises a power bus connecting said first metal pad to said second metal pad.

189. (Previously presented) The chip package in claim 179, wherein said patterned metal layer comprises a signal trace connecting said first metal pad to said second metal pad.

190. (Currently amended) The chip package in claim 179, wherein said passive device comprises ~~further comprising~~ a filter over said ~~second insulating~~ first dielectric layer.

191. (Currently amended) The chip package in claim 179, wherein said passive device comprises an inductor over said ~~second insulating~~ first dielectric layer.

192. (Currently amended) The chip package in claim 179, wherein said passive device comprises a capacitor over said ~~second insulating~~ first dielectric layer.

193. (Currently amended) The chip package in claim 179, wherein said passive device comprises a resistor over said ~~second insulating~~ first dielectric layer.

194. (Currently amended) The chip package in claim 179 further comprising a substrate under said die and under said first and second portions of said die-surrounding layer.

195. (Previously presented) The chip package in claim 194, wherein said substrate comprises silicon.

196. (Currently amended) The chip package in claim 179, wherein said passive device comprises a portion vertically over said first portion of said ~~first insulating~~ die-surrounding layer.

197. (Currently amended) A chip package comprising:

a ~~first insulating~~ die-surrounding layer;

a die between a first portion of said ~~first insulating~~ die-surrounding layer and a second portion of said ~~first insulating~~ die-surrounding layer, wherein said die has a top surface substantially coplanar with a top surface of said ~~first insulating~~ die-surrounding layer;

a ~~second insulating~~ first dielectric layer on said top surface of said die and on said top surface of said ~~first insulating~~ die-surrounding layer;

a patterned metal layer over said ~~second insulating~~ first dielectric layer, said top surface of said die and said top surface of said ~~first insulating~~ die-surrounding layer, wherein said patterned metal layer comprises a ground piece connected to a first metal pad of said die through a first opening in said ~~second insulating~~ first dielectric layer, and connected to a second metal pad of said die through a second opening in said ~~second insulating~~ first dielectric layer, wherein said first metal pad is connected to said second metal pad through said ground piece; and

a passive device over said ~~second insulating~~ first dielectric layer.

198. (Currently amended) The chip package in claim 197, wherein said passive device comprises an inductor over said ~~second insulating~~ first dielectric layer.

199. (Currently amended) The chip package in claim 197, wherein said passive device comprises a resistor over said ~~second insulating~~ first dielectric layer.

200. (Currently amended) The chip package in claim 197, wherein said ~~first insulating~~ die-surrounding layer comprises [[an]] epoxy.

201. (Currently amended) The chip package in claim 197, wherein said passive device comprises a capacitor over said ~~second insulating~~ first dielectric layer.

202. (Currently amended) The chip package in claim 197, wherein said ~~second insulating~~ first dielectric layer comprises polyimide.

203. (Currently amended) The chip package in claim 197 further comprising a ~~third insulating~~ second dielectric layer on said patterned metal layer and on said passive device.

204. (Currently amended) The chip package in claim 197, wherein said ~~second insulating~~ first dielectric layer comprises benzocyclobutene (BCB).

205. (Previously presented) The chip package in claim 197 further comprising multiple solder bumps configured for external connection.

206. (Currently amended) The chip package in claim 197 further comprising a substrate under said die and under said first and second portions of said ~~first insulating~~ die-surrounding layer.

207. (Currently amended) The chip package in claim 206, wherein said substrate comprises a silicon substrate.

208. (Currently amended) The chip package in claim 197, wherein said passive device comprises a filter over said ~~second insulating~~ first dielectric layer.

209. (Previously presented) The chip package in claim 197, wherein said patterned metal layer comprises electroplated copper.

210. (Previously presented) The chip package in claim 179, wherein said patterned metal layer comprises electroplated copper.